

## CLAIMS

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1. A method of laying out traces for connection of bond pads of a semiconductor chip to a ball grid array printed wiring board substrate or the like which comprises the steps of:

(a) providing a substrate having a surface with a plurality of rows and columns of ball pads and having a solder ball secured to said ball pads; and

(b) providing a plurality of pairs of traces on said surface, each trace of each of said pairs of traces extending to a different one of said ball pads and extending to ball pads on a plurality of said rows and columns, each trace of each of said pair of traces being spaced from the other trace of said pair by up to a ball pitch, being maximized for identity in length and having up to one ball pitch difference in length and being maximized for parallelism and spacing.

2. The method of claim 1 wherein each of said traces of said pair is further maximized for identity in cross-sectional geometry.

3. The method of claim 1 further comprising the step of applying a differential signal pair to at least one of a said pair of traces.

4. The method of claim 2 further comprising the step of applying a differential signal pair to at least one of a said pair of traces.

5. The method of claim 1 further including the step of providing a further surface insulated from said surface, a plurality of said traces being disposed on said further surface.

6. The method of claim 2 further including the step of providing a further surface insulated from said surface, a plurality of said traces being disposed on said further surface.

7. The method of claim 3 further including the step of providing a further surface insulated from said surfaces, a plurality of said traces being disposed on said further surface.

8. The method of claim 4 further including the step of providing a further surface insulated from said surface, a plurality of said traces being disposed on said further surface.

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9. A layout of traces for connection of bond pads of a semiconductor chip to a ball grid array printed wiring board substrate or the like which comprises:

(a) a substrate having a surface with a plurality of rows and columns of ball pads and having a solder ball secured to said ball pads; and

(b) a plurality of pairs of traces on said surface, each trace of each of said pairs of traces extending to a different one of said ball pads and extending to ball pads on a plurality of said rows and columns, each trace of each of said pair of traces being spaced from the other trace of said pair by up to a ball pitch, being maximized for identity in length and having up to one ball pitch difference in length and being maximized for parallelism and spacing.

10. The layout of claim 9 wherein each of said traces of said pair is further maximized for identity in cross-sectional geometry.

11. The layout of claim 9 further including means for applying a differential signal pair to at least one of a said pair of traces.

12. The layout of claim 10 further including means for applying a differential signal pair to at least one of a said pair of traces.

13. The layout of claim 9 further including a further surface between said top and bottom surfaces insulated from said top and bottom surfaces, a plurality of said traces being disposed on said further surface.

14. The layout of claim 10 further including a further surface insulated from said surface, a plurality of said traces being disposed on said further surface.

15. The layout of claim 11 further including a further surface insulated from said surface, a plurality of said traces being disposed on said further surface.

16. The layout of claim 12 further including a further surface insulated from said surface, a plurality of said traces being disposed on said further surface.

17. The method of claim 1 wherein said substrate has at least first, second and third rows and first, second, third and fourth columns of said ball pads in a matrix array, a first trace of a first pair of said traces extending to a ball pad in said first row of said second column closest to said chip and a second trace of said first pair of traces extending to a ball pad in said second row of said second column and between said first column and second column which is adjacent to said first column, a first trace of a second pair of said traces extending to a ball pad in said first row of said third column closest to said chip and a second trace of said second pair of traces extending to a ball pad in said second row of said third column and between said third column and said fourth column

